REMARKS

Claims 1-21 are pending. Claims 14-20 have been allowed. By this Response, claims 1, 6, 8 and 10 have been amended and claim 21 has been added.

The drawings have been objected to under 37 C.F.R. §1.84(p)(4) as having an improper reference character designation. Applicants are submitting a proposed drawing correction with this communication in accordance with the Examiner's suggestions. Accordingly, Applicants request that the Examiner withdraw the instant objection.

The drawings have also been objected to under 37 C.F.R. §1.83(a) as failing to show every feature of the invention specified in the claims. The aforementioned proposed drawing correction incorporates the Examiner's suggestions with regard to the identified features. Accordingly, applicants request that the Examiner withdraw the instant objection.

Claims 1-3 and 10-12 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,777,491 to Hwang et al. Applicants traverse this rejection and respectfully assert that Hwang fails to disclose all of the claimed limitations. With specific regard to claim 1, the rejected claim has been amended to include the subject matter of canceled claim 4, which has been indicated as being allowable. Applicants also point out that the newly added claim 21 represents canceled claim 5, which has been indicated as being allowable, rewritten in independent form. Claims 2, 3 and 10-12 depend from claim 1 and therefore also recite patentable subject matter.

Claims 8, 9 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hwang in view of allegedly admitted prior art of FIGS. 3 and 4. Applicants traverse this rejection and respectfully assert that Hwang and FIGS. 3 and 4 fail to establish a *prima facie* case of obviousness because all of the claimed limitations are not taught or suggested by the references. In particular, the rejected claims depend from allowable claim 1, discussed above. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

CONCLUSION

Applicants submit that the drawings and all pending claims are in condition for allowance. Accordingly, Applicants respectfully request the Examiner to pass this case to issue at the Examiner's earliest possible convenience.

The Patent Office is hereby authorized to charge any additional fees or credit any overpayment in connection with this paper to Deposit Account No. 11-0600.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (202) 220-4275.

Respectfully submitted,

Date: January 14, 2003

B. Delano Jordan
Reg. No. 43,698

Kenyon & Kenyon
1500 K Street, NW, Suite 700
Washington, D.C. 20005-1257
Tel: (202) 220-4200
Fax: (202) 220-4201

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APPENDIX A

Version with markings to show changes made

IN THE CLAIMS:

Please substitute the amended claims below for the pending claims with the same claim numbers. In the version below, deletion is shown by crossthrough and insertion is shown by underlining.

Please amend the claims as follows:

1. (Amended) A logic stage comprising:

a precharge circuit connected to a first potential and a differential output defined by a first output node and a second output node;

a first evaluate circuit connected to a second potential and the first output node; and

a second evaluate circuit connected to the second potential and the second output node, the second evaluate circuit being symmetric with the first evaluate circuit, each evaluate circuit including a transistor stack connected between the second potential and one of the output nodes, and an input transistor connected in parallel with the transistor stack, each transistor stack including a first series transistor connected to the second potential, and a second series transistor connected between the first series transistor and one of the output nodes, the first series transistor being larger than the second series transistor.

6. (Amended) The logic stage of claim 21 ~~5~~ wherein the second series transistor is to receive a generate input corresponding to a less significant bit ~~of an added circuit~~, the first series transistor and input transistor to receive inputs corresponding to a more significant bit.

8. (Amended) The logic stage of claim 1 ~~2~~ wherein the evaluate circuits include PMOS transistors.

10. (Amended) The logic stage of claim 1 ~~2~~ wherein the evaluate circuits include NMOS transistors.